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U.S. **UTILITY** Patent Application

PATENT NUMBER and ISSUE DATE

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10072533	02/08/2002	333		2817	

**APPLICANTS: Ishikawa Yohei; Sakamoto Koichi; Yamashita Sadao; Iio Kenichi;

12-4/19/16

**CONTINUING DATA VERIFIED:
THIS APPLICATION IS A DIV OF 09/031,981 02/26/1998 6195255

** FOREIGN APPLICATIONS VERIFIED:
JAPAN 9-44162 02/27/1997

PG-PUB DO NOT PUBLISH ☐ | RESCIND ☐

Foreign priority claimed ☑ yes ☐ no
35 USC 119 conditions met ☑ yes ☐ no
Verified and Acknowledged Examiners's initials

ATTORNEY DOCKET NO
P/1071-1520

TITLE : Planar dielectric integrated circuit

U.S DEPT. OF COMM./PAT. & TM-PTO-436L(Rev. 10-94)

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED	
			Total Claims	Print Claim for O.G
ISSUE FEE			DRAWING	
Amount Due	Date Paid		Sheets Drwg.	Figs.Drwg. / Print Fig. 7
☐ TERMINAL DISCLAMER		Primary Examiner	Application Examiner	
		PREPARED FOR ISSUE		

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(Attached in pocket on right inside flap)